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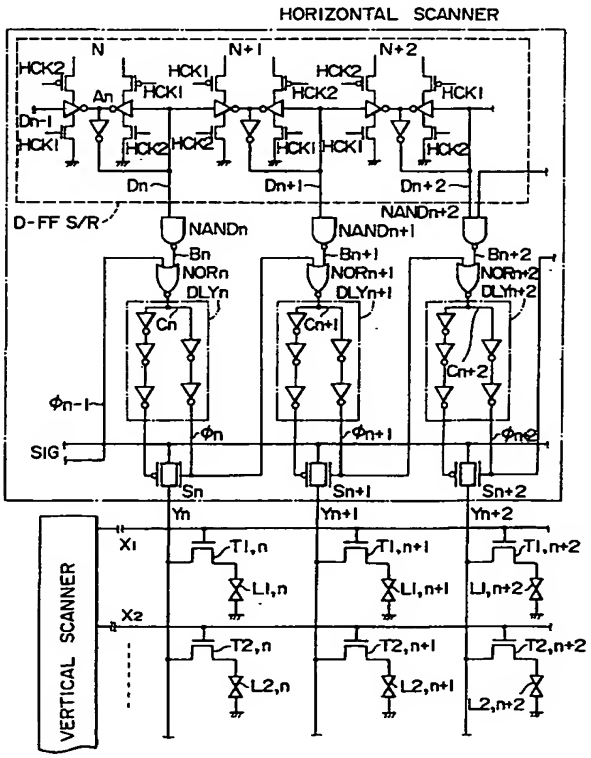
(54) Horizontal driver circuit with fixed pattern eliminating function.

(57) A horizontal driver circuit comprising a shift register for generating horizontal sampling pulses sequentially; and a fixed pattern eliminating circuit, associated with the shift register, for providing a non-overlap time of the horizontal sampling pulses between an Nth stage and an Mth stage posterior thereto. The Mth stage horizontal sampling pulse has a rise whose phase is the same as that of a fall of the Nth stage horizontal sampling pulse. The fixed pattern eliminating circuit comprises means for controlling the rise of the horizontal sampling pulse of the Mth stage by the fall of the horizontal sampling pulse of the Nth stage. The horizontal driver circuit is applicable to a two-dimensional addressing device and a liquid crystal display device to eliminate a fault of vertical streaks on a displayed image.

FIG. 1



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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an active matrix type liquid crystal display device comprising active elements such as thin film transistors disposed at intersections of gate lines and data lines in a matrix array, and picture element electrodes corresponding to such active elements. And more particularly, the invention relates to a horizontal driver circuit for distributively supplying video signals to data lines in a line sequential mode.

Description of the Prior Art

For the purpose of making the present invention better understood with facility, there is shown in Fig. 8 a general equivalent circuit representing the background prior art in an active matrix type liquid crystal display device. As shown, the liquid crystal display device of such type comprises a plurality of gate lines X1, X2, ... arranged in parallel with one another in the X-axis direction; and a plurality of data lines Y1, Y2, ... arranged in parallel with one another in the Y-axis direction. Active elements such as thin film transistors (TFTs) T11, T12, T21, T22, ... are disposed at the intersections of the gate lines and the data lines. And liquid crystal cells L11, L12, L21, L22, ... are also disposed correspondingly to the thin film transistors. Gate electrodes of the TFTs are connected respectively to the gate lines while source electrodes thereof are connected respectively to the data lines, and drain electrodes thereof are connected respectively to picture element electrodes of the corresponding liquid crystal cells. Each of the liquid crystal cells is composed of liquid crystal held between one picture element electrode and a common electrode COM opposed thereto.

The data lines Y1, Y2, ... are connected via corresponding switching transistors S1, S2, ... respectively to a common signal line SIG, to which a video signal is supplied from an external source. And a horizontal driver circuit is connected to the gate electrode of each switching transistor. The horizontal driver circuit sequentially feeds horizontal switch driving pulses $\phi 1$, $\phi 2$, ... to the gate electrodes of the switching transistors in synchronism with horizontal clock pulses HCLK inputted from an external source. Meanwhile the gate lines X1, X2, ... are connected to an unshown vertical driver circuit.

Now the operation of the circuit shown in Fig. 8 will be briefly described below. When an unshown vertical driver circuit is actuated, the gate lines are sequentially excited so that the TFTs are selected row by row. If the horizontal driver circuit is actuated at this time to operate the switching transistors line-sequentially, the video signals supplied to the signal line SIG are sequentially sampled at the data lines. The video signals thus sampled are sequentially written in the corresponding liquid crystal cells via the TFTs selected row by row. In this manner, the data of the sampled video signals are written dot-sequentially in the individual liquid crystal cells.

Next the problems to be solved by the present invention will be described briefly with reference to Fig. 9. The horizontal driver circuit shown in Fig. 8 comprises a shift register and so forth and sequentially produces horizontal switch driving pulses $\phi 1$, $\phi 2$, ... as output signals. This driver circuit is so designed that the preceding pulse $\phi 1$ and the succeeding pulse $\phi 2$ generated therefrom do not overlap mutually with regard to logic levels. Practically, however, there occurs a partial overlap due to some jitter derived from waveform distortion or the like in the leading and trailing edges of the pulses. In other words, the mutually adjacent pulses interfere with each other. The quantity of such jitter is inherent in and dependent on the electric characteristics of the individual device in each stage of the shift register. Therefore the overlap pattern between pulse trains is fixed, and a specific quantity of jitter tends to appear continuously in a specific stage of the shift register.

As described above, first the switching transistor S1 is turned on in response to the preceding pulse $\phi 1$, and then the video signal from the common signal line SIG is sampled at the corresponding data line Y1. Subsequently the switching transistor S2 is turned on in response to the succeeding pulse $\phi 2$, and the video signal from the common signal line SIG is sampled at the corresponding data line Y2. However, if any jitter is existent at this time, the succeeding pulse $\phi 2$ rises or turns on before a fall of the preceding pulse $\phi 1$, so that a potential fluctuation is caused in the signal line SIG by the charge-discharge current during such period of time. Since the potential fluctuation is induced prior to the fall of the preceding pulse, it is sampled at the data line Y1 to consequently bring about an error in the sample data of the data line Y1. As this error depends on the jitter quantity, it follows that the error appears continuously in a specific stage where the jitter quantity is particularly great. On the whole display screen, such error is seen like a vertical streak to eventually raise a problem that the image quality is extremely deteriorated. Generally a video driver for outputting a video signal to the signal line SIG has a high output impedance and, since the impedance of the signal line is also high, harmful influence is considerably exerted by the jitter of the horizontal switch driving pulses to eventually render conspicuous the verti-

cal streak or fixed overlap pattern on the displayed image. Furthermore, if the so-called simultaneous R-G-B driving is performed in an attempt to reduce the power consumption while lowering the clock pulse frequency for the horizontal driver circuit, the apparent number of columns of picture elements is decreased to consequently worsen the drawbacks relative to vertical streaks.

OBJECT AND SUMMARY OF THE INVENTION

The present invention has been accomplished in view of the above problems observed in the prior art. And it is an object of the invention to provide an improved horizontal driver circuit which is employed in an active matrix type liquid crystal display device and is equipped with a fixed overlap pattern eliminating function so as to remove the aforementioned fault of vertical streaks on a displayed image.

According to one aspect of the present invention, there is provided a horizontal driver circuit comprising a shift register for generating horizontal sampling pulses sequentially; and a fixed pattern eliminating circuit, associated with the shift register, for providing a non-overlap time of the horizontal sampling pulses between an Nth stage and an Mth stage posterior thereto. The Mth stage horizontal sampling pulse has a rise whose phase is the same as that of a fall of the Nth stage horizontal sampling pulse. The fixed pattern eliminating circuit comprises means for controlling the rise of the horizontal sampling pulse of the Mth stage by the fall of the horizontal sampling pulse of the Nth stage.

According to another aspect of the present invention, there is provided an addressing device comprising a plurality of gate lines arranged substantially in parallel with each other in the X-axis direction; a plurality of data lines arranged substantially in parallel with each other in the Y-axis direction; a first scanning means for supplying gate signals sequentially to the gate lines; a second scanning means for supplying data signals sequentially to the data lines, the second scanning means comprising a shift register for sequentially generating horizontal sampling pulses, a fixed pattern eliminating circuit associated with the shift register, a delay circuit for delaying outputs from the fixed pattern eliminating circuit, and switch elements for providing data signals to the data lines in response to outputs from the delay circuit; and active elements disposed at intersecting points of the gate and data lines. The fixed pattern eliminating circuit serves to provide a non-overlap time of the horizontal sampling pulses between an Nth stage and an Mth stage posterior thereto, and the Mth stage horizontal sampling pulse has a rise whose phase is the same as that of a fall of the Nth stage horizontal sampling pulse.

According to a further aspect of the present invention, there is provided a liquid crystal display device comprising a plurality of display elements arranged in a matrix, each display element comprising a picture element electrode and a switching element associated with the picture element electrode, the switching element having first and second electrodes, a plurality of gate lines associated with the first electrode; a plurality of data lines associated with the second electrodes; and a scanning circuit having a control means for generating a non-overlap time of horizontal sampling pulses so that the rise of an Mth pulse is controlled by the fall of an Nth pulse, the rise of the Mth pulse being substantially the same in phase as the fall of the Nth pulse, to thereby sample video signals to be sequentially supplied to the data lines.

In the present invention, a fixed pattern eliminating circuit is connected to the output of the shift register for sequentially generating horizontal sampling pulses. Such fixed pattern eliminating circuit controls, by the use of an Nth stage preceding horizontal sampling pulse as a control signal, the output timing of the Mth stage succeeding horizontal sampling pulse whose rise is the same in phase as the fall of the Nth stage preceding horizontal sampling pulse. In other words, the output of the succeeding pulse is inhibited during the output of the preceding pulse so that the succeeding pulse rises exactly after the fall of the preceding pulse. Furthermore, the succeeding pulse outputted from the fixed pattern eliminating circuit is supplied, after delay of a predetermined time, to a corresponding video signal sampling switch. As a result, there never occurs an overlap between the preceding sample corresponding to the Nth stage in the shift register and the succeeding sample corresponding to the Mth stage therein, whereby a fault of vertical streak or a fixed overlap pattern can be eliminated. In the present invention where a preceding pulse is used for controlling the output timing of a succeeding pulse, it becomes possible to remove the necessity of adding any circuit of a complicated configuration or a clock pulse source either.

The above and other features and advantages of the present invention will become apparent from the following description which will be given with reference to the illustrative accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of an exemplary active matrix type liquid crystal display device where the horizontal driver circuit of the present

invention is applied;

Fig. 2 is a timing chart of signals for explaining the operation of the horizontal driver circuit shown in Fig. 1;

Fig. 3 is another timing chart of signals for explaining the operation of the horizontal driver circuit shown in Fig. 1;

Fig. 4 is a circuit diagram of an exemplary modification of a fixed pattern eliminating circuit included in the horizontal driver circuit of Fig. 1;

Fig. 5 is a circuit diagram of another embodiment representing the horizontal driver circuit of the invention;

Fig. 6 is a timing chart of signals for explaining the operation of the horizontal driver circuit shown in Fig. 5;

Fig. 7 is a timing chart of signals for explaining the operation of an exemplary modification of the horizontal driver circuit shown in Fig. 5;

Fig. 8 is a circuit diagram of a conventional active matrix type liquid crystal display device; and Fig. 9 is a timing chart of signals for explaining the problems in the conventional device of Fig. 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings. Fig. 1 is a typical circuit block diagram in an exemplary case of applying the present invention to an active matrix type liquid crystal display device. It is to be understood that the present invention is generally applicable to a two-dimensional addressing device as well without being limited merely to such two-dimensional display device alone.

As shown, the display device comprises a plurality of gate lines X1, X2, ... arranged in parallel with one another in the X-axis direction, a plurality of data lines Yn, Yn+1, Yn+2, ... arranged in parallel with one another in the Y-axis direction, a first scanner or vertical scanner for supplying gate signals line-sequentially to the gate lines, and a second scanner or horizontal scanner for supplying video signals line-sequentially to the data lines.

Active elements such as thin film transistors (TFTs) $T_{1,n}$, $T_{1,n+1}$, $T_{1,n+2}$, $T_{2,n}$, $T_{2,n+1}$, $T_{2,n+2}$ ... are disposed respectively at the intersections of the gate lines and the data lines. And liquid crystal cells $L_{1,n}$, $L_{1,n+1}$, $L_{1,n+2}$, $L_{2,n}$, $L_{2,n+1}$, $L_{2,n+2}$, ... are connected respectively to the individual TFTs. Each of the liquid crystal cells is composed of a picture element electrode, a common electrode opposed thereto, and a liquid crystal layer held between the two electrodes. Drain electrodes of the TFTs are connected to the picture element electrodes, while gate electrodes thereof are connected to the corresponding gate lines, and source electrodes thereof are connected to the corresponding data lines. The TFTs are selected row by row in accordance with the gate signals supplied from the gate lines and, after dot-sequentially accessing the video signals supplied from the data lines, writes the video signals in the corresponding liquid crystal cells.

Such picture element electrodes, TFTs, gate lines, data lines, vertical scanner and horizontal scanner are so arrayed as to form a matrix on one substrate, although not shown, by the semiconductor process. Meanwhile the common electrode is provided on another substrate. An active matrix type liquid crystal display device can be constituted by holding a liquid crystal layer between the two substrates opposed to each other via a predetermined space retained therebetween.

The circuit configuration of the horizontal scanner, which is a principal component in the present invention, will now be described below in detail with further reference to Fig. 1. The horizontal scanner has a shift register S/R where a multiplicity of stages of n-type flip-flops (D-FF) are connected. For the purpose of simplifying the diagram, merely its Nth stage through (N+2)th stage are extracted and shown. A NAND element is connected to the output of each stage in the shift register. Here, a suffix is added to a reference symbol NAND for representing the correlation to each stage in the shift register. For example, a NAND element connected to the Nth stage output terminal is expressed as NANDn. In the following description, similar suffixes will be used also with regard to any other kinds of elements and signal pulses in conformity to the above rule when there is the necessity of representing the correlation to the stages in the shift register. Horizontal sampling pulses B are sequentially outputted from the NAND elements. These sampling pulses will be termed "primary pulses B" below since such pulses still contain some jitter prior to elimination of the fixed overlap pattern.

A NOR element is connected to the output terminal of each NAND element. A group of such NOR elements constitute a fixed pattern eliminating circuit. Furthermore a delay element DLY is connected to the output terminal of each NOR element. And a group of such delay elements constitute a delay circuit. From the output terminal of the delay circuit, there are delivered horizontal sampling pulses ϕ posterior to elimination of the jitter and a predetermined delay process. Hereinafter such pulses already processed as mentioned will be termed "secondary pulses ϕ". Practically, the output signal of the delay element DLY includes secondary pulses ϕ and inverted pulses

thereof. A transmission gate element S is connected to a pair of output terminals of the delay element. And a group of the transmission gate elements constitute switch means. The input terminals of the transmission gate elements are connected to a common signal line SIG through which video signals are supplied, and the output terminals thereof are connected respectively to the corresponding data lines Y. The transmission gate elements are turned on merely during the supply of the secondary pulses ϕ thereto, so that the video signals are supplied and transferred sequentially to the corresponding data lines Y.

The primary pulses B are supplied as described to one input terminal of each NOR element constituting the fixed pattern eliminating circuit, while the secondary pulses ϕ are supplied to the other input terminal thereof. The NOR element controls, by using the preceding secondary pulse ϕ as a control signal, the output timing of the succeeding primary pulse B whose rise is the same in phase as the fall of the preceding secondary pulse. In this embodiment, the rise timing of the next-stage primary pulse B is controlled in accordance with the preceding-stage secondary pulse ϕ. For example, the Nth stage element NORn executes gate control of the primary pulse Bn in accordance with the secondary pulse ϕn-1.

In this embodiment, each delay element DLY constituting the delay circuit consists of series-connected inverters. A desired delay time is attainable by setting the number of connected inverters to an adequate value. It is to be noted here that there occurs a predetermined delay in the NOR element as well. Consequently, the total delay time in the entire circuit is the sum of the delay in the NOR element and that in the delay element DLY.

Now the operation of the horizontal scanner shown in Fig. 1 will be described below in detail with reference to Figs. 2 and 3. Referring first to the timing chart of Fig. 2, a description will be given on how a primary pulse B is outputted from the shift register S/R. A data pulse Dn-1 is transferred from the preceding stage to the Nth stage D-FF of the shift register S/R. Meanwhile a horizontal clock signal HCK1 and its inverted signal HCK2 are supplied to each stage in the shift register. In this embodiment, the width of the data pulse D is set to a duration equal to one period of the clock signal. The data pulse Dn-1 inputted from the preceding stage to the Nth stage in the shift register is delayed by a time length equal to half the period of the clock signal and is inverted by the paired inverters. In Fig. 2, An represents the waveform of the pulse thus processed. The pulse An is further inverted by another inverter so that an Nth stage data pulse Dn is obtained. As obvious from the timing chart, the data pulse Dn is shifted, in comparison with the preceding stage data pulse Dn-1, by a time length equal to half the period of the clock signal. In this manner, data pulses Dn, Dn + 1, Dn + 2, ... and so forth, each shifted by half the period of the clock signal, are sequentially outputted from the shift register S/R.

NAND elements are connected respectively to the output terminals of the individual stages in the shift register. For example, the element NANDn connected to the Nth stage produces a primary pulse Bn as an output by executing a NAND process of the Nth stage data pulse Dn and the next stage data pulse Dn + 1. Similarly, the element NANDn + 1 connected to the (N + 1)th stage output terminal produces a next primary pulse Bn + 1. Each of the primary pulses B thus outputted sequentially has a duration equal to half the period of the clock signal and is shifted by a time length equal to the pulse duration thereof. In other words, the next stage primary pulse is outputted immediately after the output of the preceding stage primary pulse. The primary pulses sequentially outputted in this manner do not overlap each other in respect of the logic levels. Practically, however, some jitter is induced due to waveform distortion in the rise and the fall of the pulses to consequently cause a mutual overlap.

Hereinafter the operation of producing secondary pulses ϕ will be described with reference to the timing chart of Fig. 3. As mentioned, the element NORn constituting a fixed pattern eliminating circuit is connected to the Nth stage element NANDn. The element NORn produces a pulse Cn as an output by executing a NOR process of the Nth stage primary pulse Bn and the preceding stage secondary pulse ϕn-1. As obvious from the timing chart of Fig. 3, the pulse Cn rises or turns on in synchronism with the fall of the preceding stage secondary pulse ϕn-1. Therefore, even if some jitter is included in the Nth stage primary pulse Bn, such jitter can be eliminated from the corresponding pulse Cn. This pulse Cn is delayed by a predetermined time length through the delay element DLYn to become a final secondary pulse ϕn. In this manner, the fixed pattern eliminating circuit controls, by using the preceding secondary pulse as a control signal, the output timing of the succeeding secondary pulse whose rise is the same in phase as the fall of the preceding secondary pulse, thereby eliminating the fixed overlap pattern. There never occurs any mutual overlap between the secondary pulses ϕn-1, ϕn, ϕn + 1, ... and so forth thus outputted sequentially after the process mentioned, hence solving the problem of vertical streak on the displayed image observed in the prior art.

Fig. 4 shows an exemplary modification of the aforementioned circuit of Fig. 1. For the purpose of

making this modified circuit better understood with facility, the Nth stage of the horizontal scanner is extracted and shown. In Fig. 4, the same component elements as those employed in the circuit of Fig. 1 are denoted by the same reference numerals or symbols. The different point resides in that the fixed pattern eliminating circuit comprises a combination of an inverter I and a NAND element. The fixed pattern eliminating circuit of such configuration has the same function as that of the aforementioned fixed pattern eliminating circuit (NORn).

Now another embodiment representing the horizontal scanner or driver of the present invention will be described below with reference to Fig. 5. In an attempt to facilitate the understanding, the same component elements as those employed in the circuit of Fig. 1 are denoted by the same reference numerals or symbols. The difference from the foregoing embodiment of Fig. 1 resides in that the NAND elements connected respectively to the output terminals of the individual stages in the shift register S/R are not employed. Therefore, in this embodiment, data pulses D outputted from the respective stages in the shift register are fed directly to the corresponding NOR elements. And in relation thereto, the secondary pulses ϕ from the ante-preceding stage is fed to the other input terminal of each NOR element, instead of the secondary pulse ϕ from the immediately preceding stage.

Referring next to Fig. 6, a description will be given on the operation of the horizontal driver circuit shown in Fig. 5. As mentioned above, the shift register S/R sequentially outputs data pulses D each having a duration equal to one period of the clock signal HCK. The data pulses are mutually shifted by a time length equal to half the period of the clock signal. In this embodiment, the data pulses are divided into two groups. One group includes data pulses Dn, Dn + 2, Dn + 4, ... of the even-numbered stages, while another group includes data pulses Dn + 1, Dn + 3, Dn + 5, ... of the odd-numbered stages. The data pulses of the even-stage group and those of the odd-stage group are used for sampling the video signals supplied from mutually different signal lines. In the same group, there may occur interference between the pulses due to the existence of some jitter. For this reason, the secondary pulse of the ante-preceding stage, instead of that of the immediately preceding stage, is used as a control signal for controlling the rise timing of the succeeding stage pulse. In the present invention, as mentioned, the preceding pulse is generally used as a control signal for controlling the output timing of any specific succeeding pulse which has a possibility of causing pulse interference, and such specific succeeding pulse is not limited merely to the next pulse alone as shown in Fig. 1.

The situation to control the pulse generation timing with a time interval as mentioned above is induced in an exemplary case of Fig. 7 as well. In this example, the width of the data pulse D transferred in the shift register is set to a long duration which is equal to two periods of the clock signal HCK. In this case also, the shift register sequentially outputs data pulses Dn, Dn + 1, Dn + 2, Dn + 3, Dn + 4, Dn + 5, ... which are mutually shifted by a time length equal to half the period of the clock signal. As obvious from the timing chart of Fig. 7, pulse interference or bit interference occurs at an interval of three stages. Since the rise timing of, e.g., the succeeding data pulse Dn + 4 is the same in phase as the fall timing of the preceding data pulse Dn, there exists a possibility of bit interference between such two pulses. In this case, therefore, the horizontal sampling pulse preceding by four stages is used as a control signal for controlling the output timing of the horizontal sampling pulse of the succeeding stage.

According to the present invention, as described hereinabove, there is attainable an advantageous effect that vertical streaks on a displayed image can be eliminated by incorporating a fixed pattern eliminating circuit in a horizontal driver circuit. The fixed pattern eliminating circuit has a relatively simplified configuration where the output timing of a succeeding pulse is controlled by the use of a preceding pulse, and the circuit function is not effected harmfully by any electric characteristic variations of the devices in the individual stages. And remarkable effects can be achieved particularly in the case of applying the horizontal driver circuit, which is equipped with such fixed overlap pattern eliminating function, in an active matrix type liquid crystal display device based on the simultaneous R-G-B driving system.

Claims

1. A horizontal driver circuit comprising:

   a shift register for generating horizontal sampling pulses sequentially; and

   a fixed pattern eliminating circuit, associated with the shift register, for providing a non-overlap time of the horizontal sampling pulses between an Nth stage and an Mth stage which follows the Nth stage, said Mth stage horizontal sampling pulse having a rise the phase of which is the same as that of a fall of the Nth stage horizontal sampling pulse.

2. A horizontal driver circuit as claimed in claim 1, wherein said fixed pattern eliminating circuit comprises means for controlling the rise of the horizontal sampling pulse of the Mth stage by

the fall of the horizontal sampling pulse of the Nth stage.

3. A horizontal driver circuit as claimed in claim 1, wherein said Mth stage is an (N + 1)th stage.

4. A horizontal driver circuit as claimed in claim 1, wherein said Mth stage horizontal sampling pulse rises by utilizing the Nth stage horizontal sampling pulse.

5. A horizontal driver circuit as claimed in claim 2, wherein said controlling means comprises NOR elements.

6. A horizontal driver circuit as claimed in claim 2, wherein said controlling means comprises a plurality of inverters and NAND elements coupled to the inverters.

7. An addressing device comprising:

a plurality of gate lines arranged substantially in parallel with each other in the X-axis direction;

a plurality of data lines arranged substantially in parallel with each other in the Y-axis direction;

a first scanning means for supplying gate signals sequentially to the gate lines;

a second scanning means for supplying data signals sequentially to the data lines, said second scanning means comprising a shift register for sequentially generating horizontal sampling pulses, a fixed pattern eliminating circuit associated with the shift register, a delay circuit for delaying outputs from the fixed pattern eliminating circuit, and switch elements for providing data signals to the data lines in response to outputs from the delay circuit, said fixed pattern eliminating circuit providing a non-overlap time of the horizontal sampling pulses between an Nth stage and an Mth stage which follows the Nth stage, said Mth stage horizontal sampling pulse having a rise the phase of which is the same as that of a fall of the Nth stage horizontal sampling pulse; and

active elements disposed at intersecting points of the gate and data lines.

8. An addressing device as claimed in claim 7, wherein said fixed pattern eliminating circuit comprises means for controlling the rise of the horizontal sampling pulse of the Mth stage by the fall of the horizontal sampling pulse of the Nth stage.

9. An addressing device as claimed in claim 7, wherein said Mth stage is an (N + 1)th stage.

10. An addressing device as claimed in claim 7, wherein said delay circuit and switch element comprise a complementary pulse generator.

11. An addressing device as claimed in claim 7, wherein said active elements comprise thin film transistors.

12. An addressing device as claimed in claim 8, wherein said switch element comprises a CMOS transmission gate.

13. A liquid crystal display device comprising:

a plurality of display elements arranged in a matrix, each display element comprising a picture element electrode and a switching element associated with the picture element electrode, said switching element having first and second electrodes;

a plurality of gate lines associated with the first electrodes;

a plurality of data lines associated with the second electrodes; and

a scanning circuit having a control means for generating a non-overlap time of horizontal sampling pulses so that the rise of an Nth pulse is controlled by the fall of an Nth pulse, said rise of the Mth pulse being substantially the same in phase as the fall of the Nth pulse, to thereby sample video signals to be sequentially supplied to the data lines.

14. A liquid crystal display device as claimed in claim 13, wherein said Mth pulse is an (N + 1)-th pulse.

FIG. 1

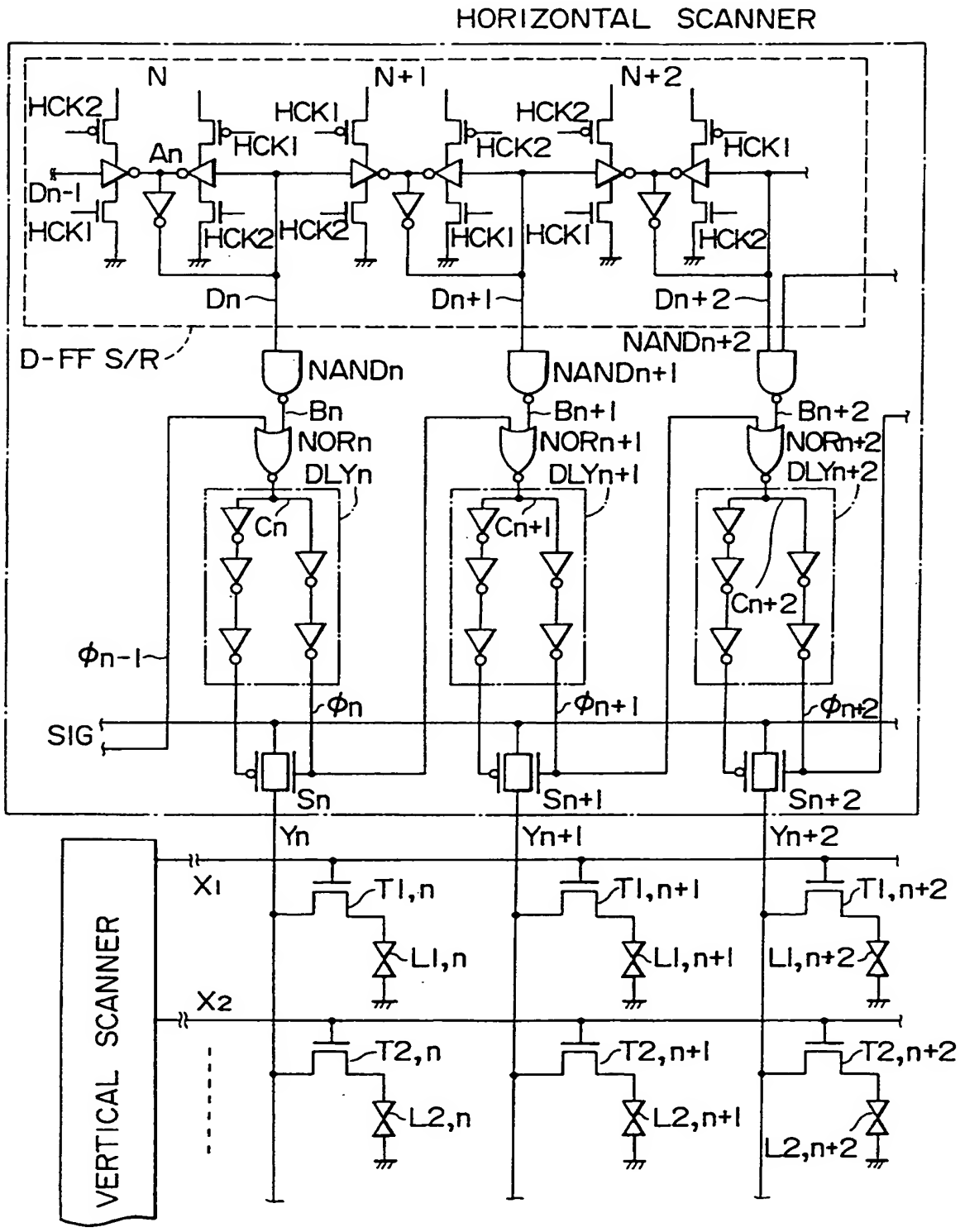
HORIZONTAL SCANNER
N
N+1
N+2
HCK2
HCK1
An
Dn-1
Dn
Dn+1
Dn+2
D-FF S/R
NANDn
NANDn+1
NANDn+2
Bn
Bn+1
Bn+2
NORn
NORn+1
NORn+2
DLYn
DLYn+1
DLYn+2
Cn
Cn+1
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FIG. 2

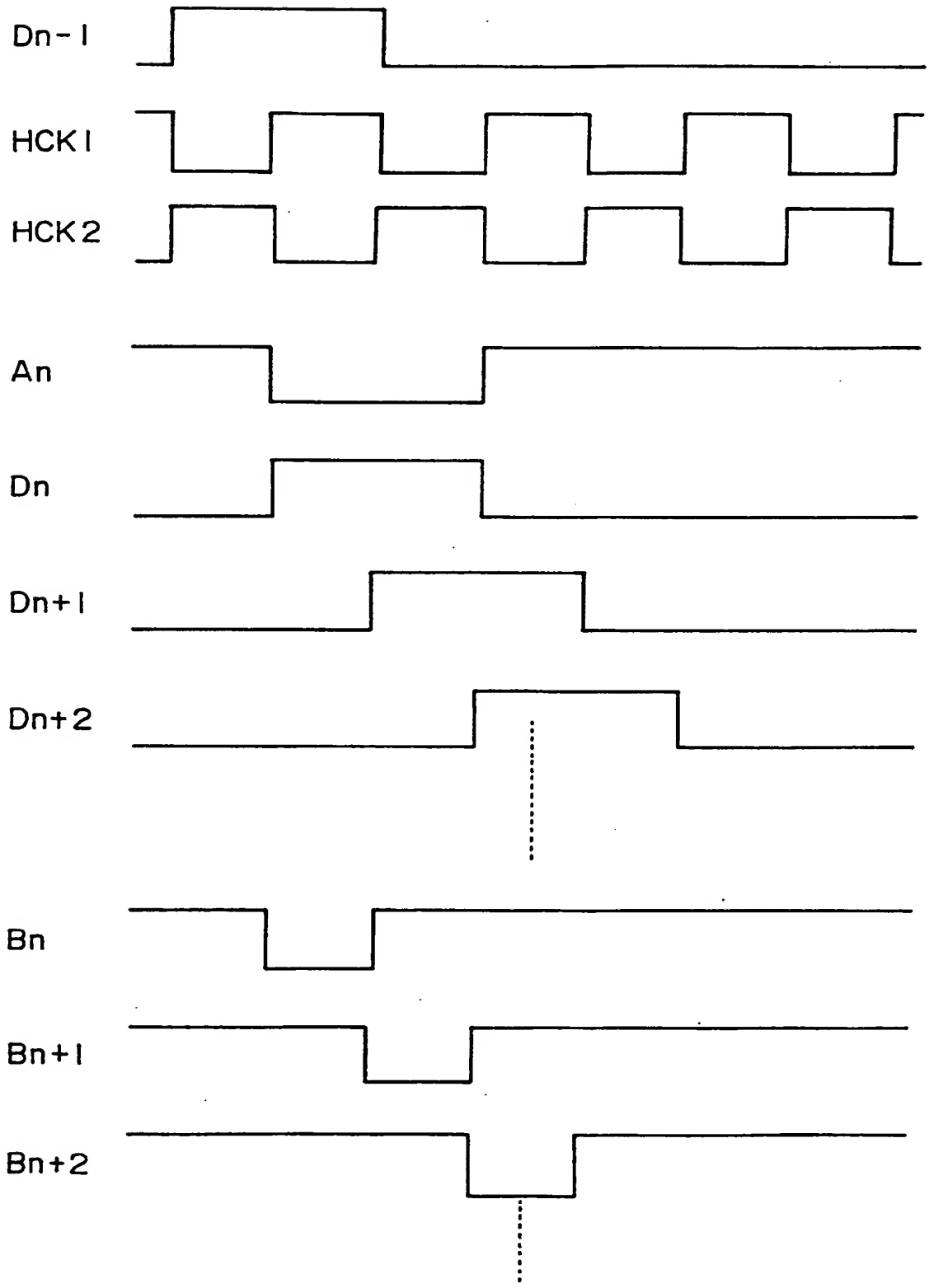


FIG. 3

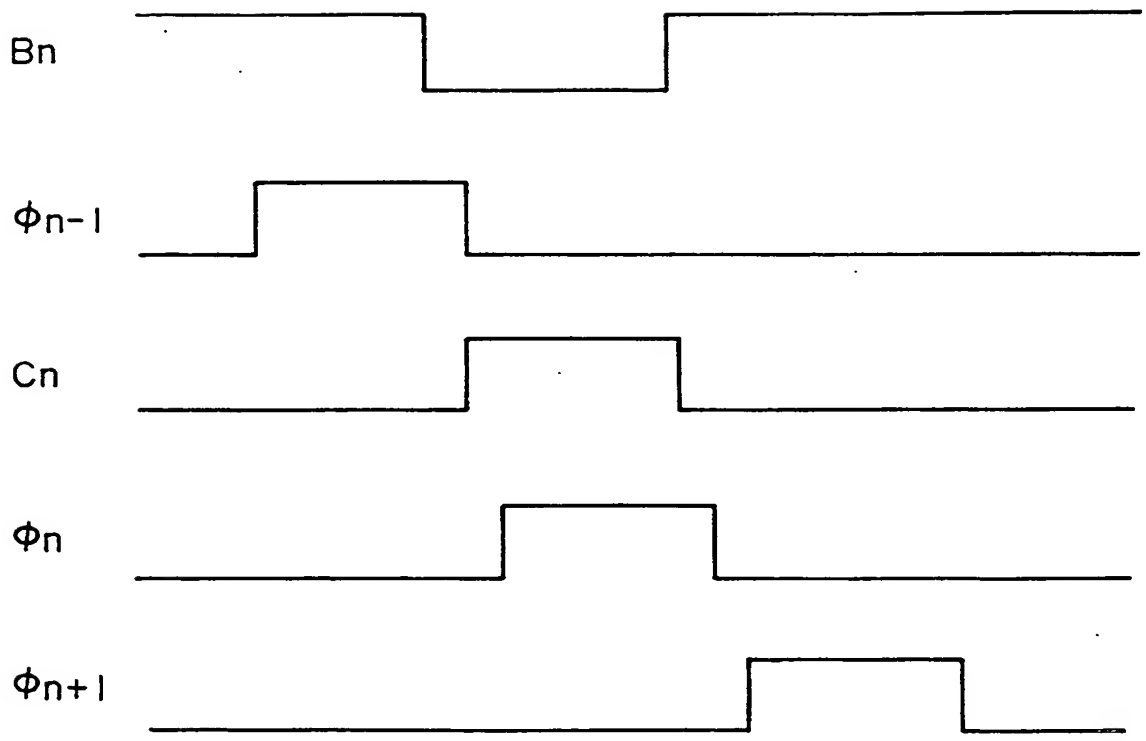


FIG. 4

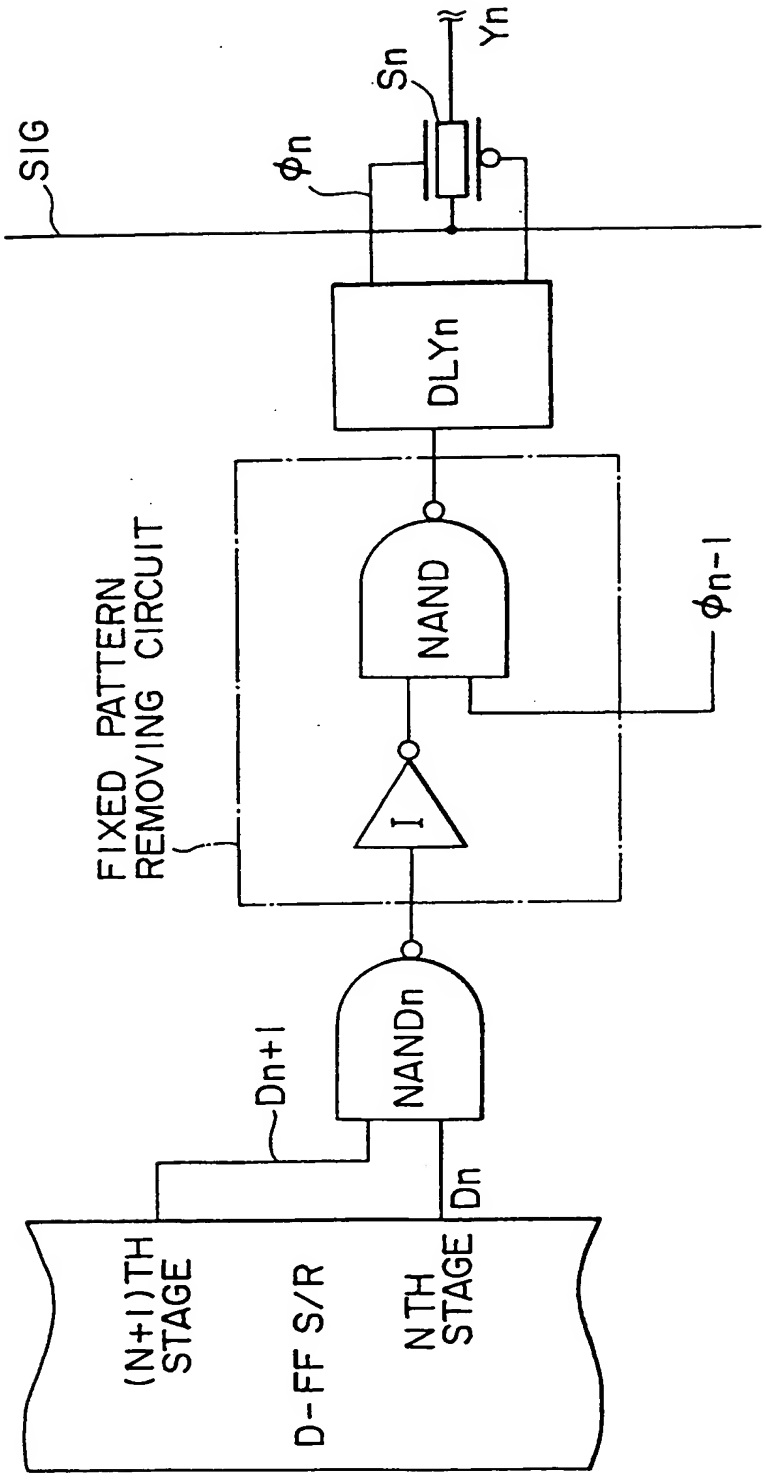
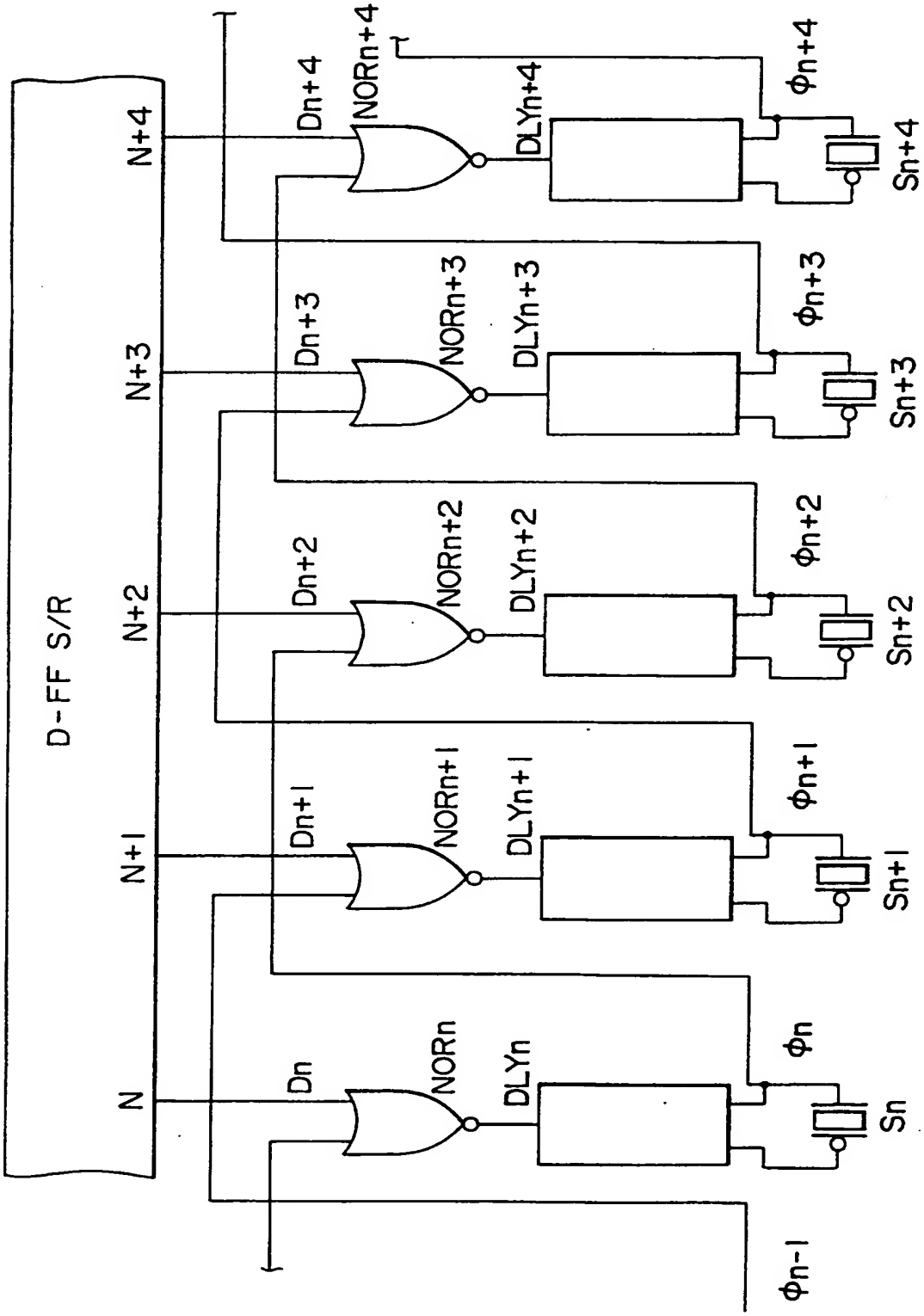

SIG
φn
Sn
Yn
DLYn
NAND
φn-1
I
FIXED PATTERN
REMOVING CIRCUIT
NANDn
Dn+1
Dn
(N+1)TH
STAGE
D-FF S/R
NTH
STAGE

FIG. 5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Sn+3
Sn+4

FIG. 6

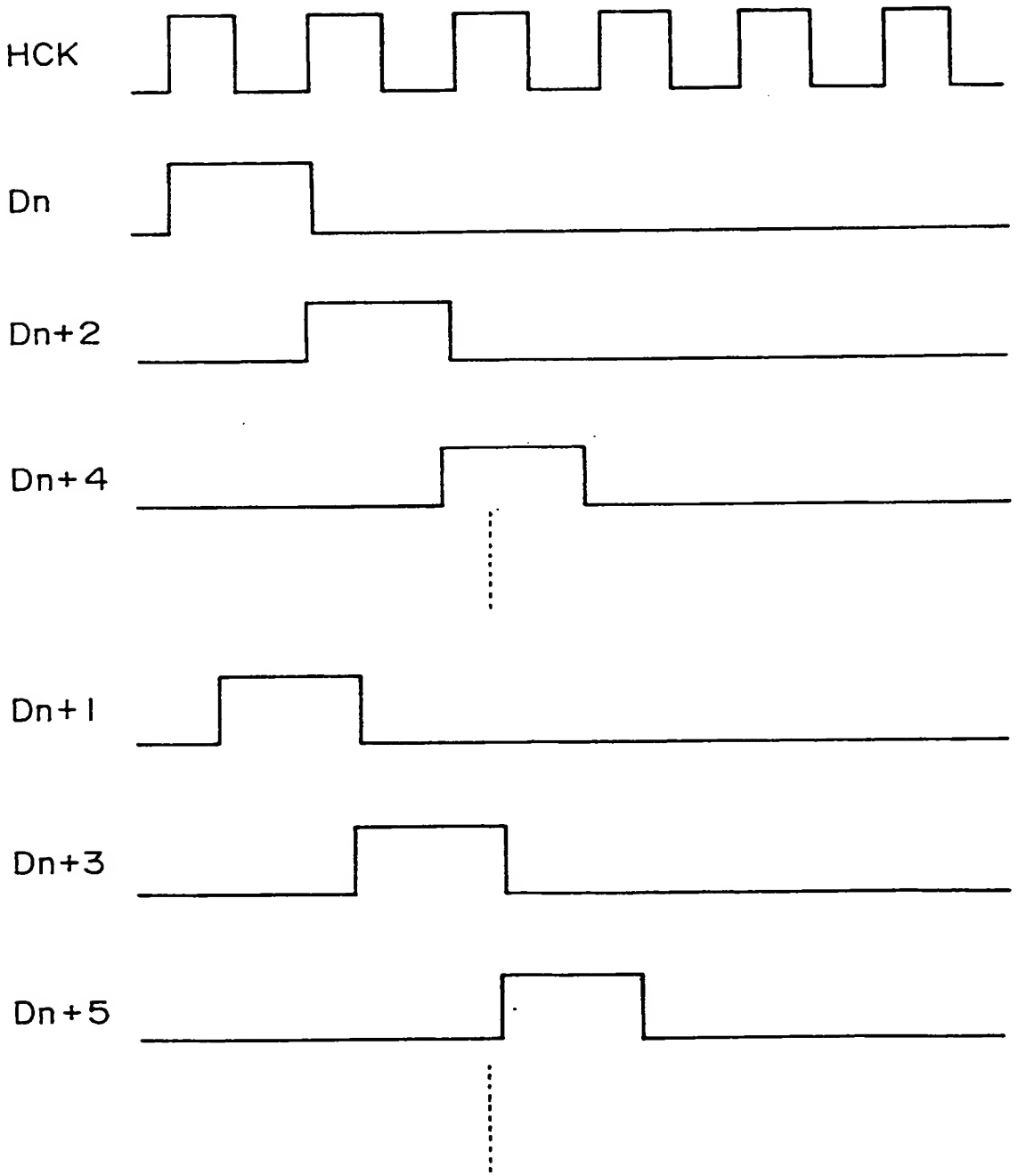


FIG. 7

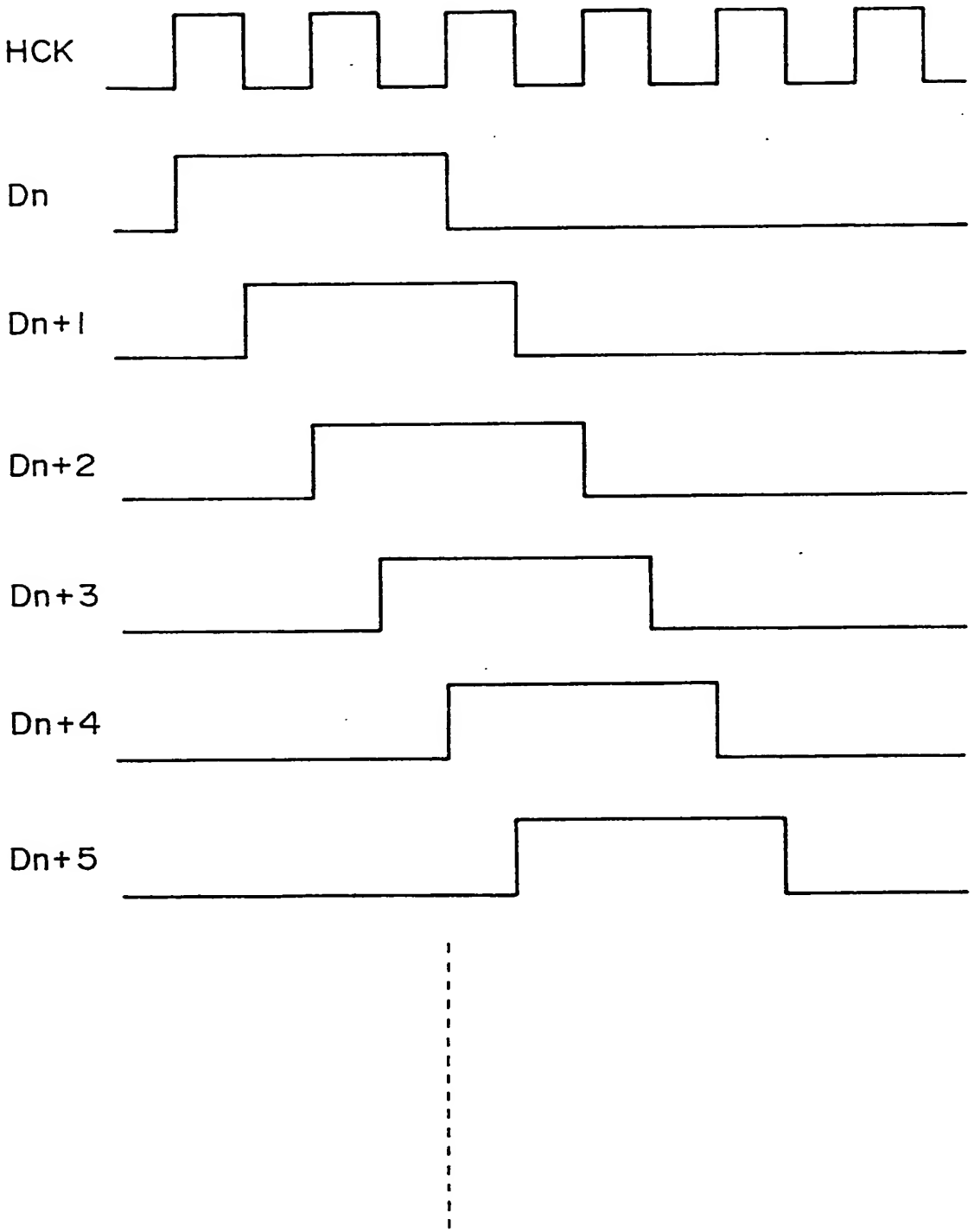


FIG. 8

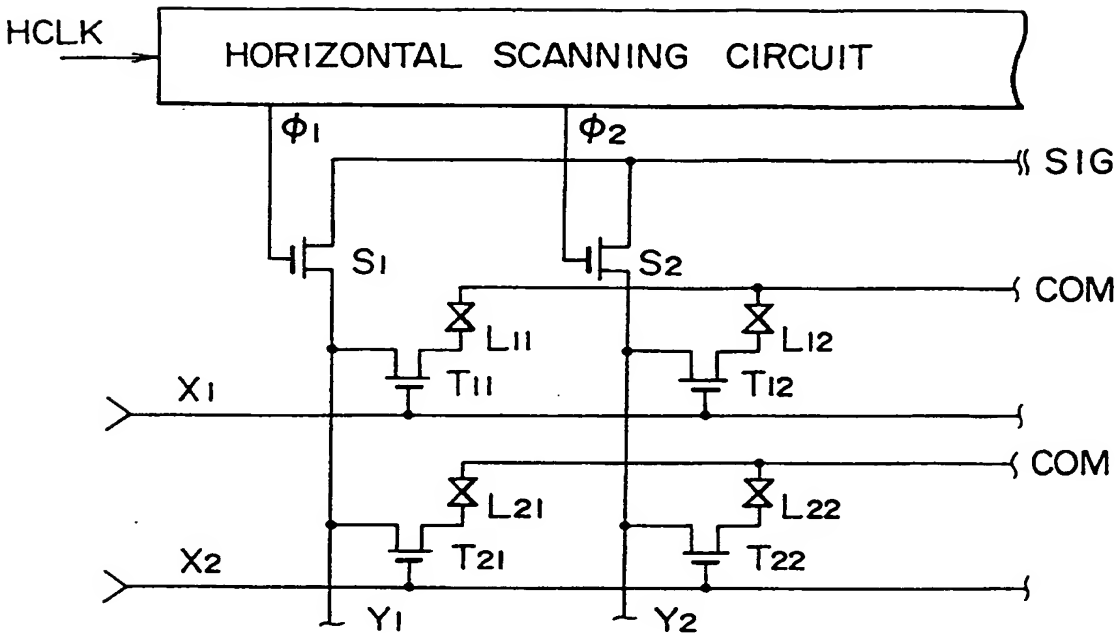
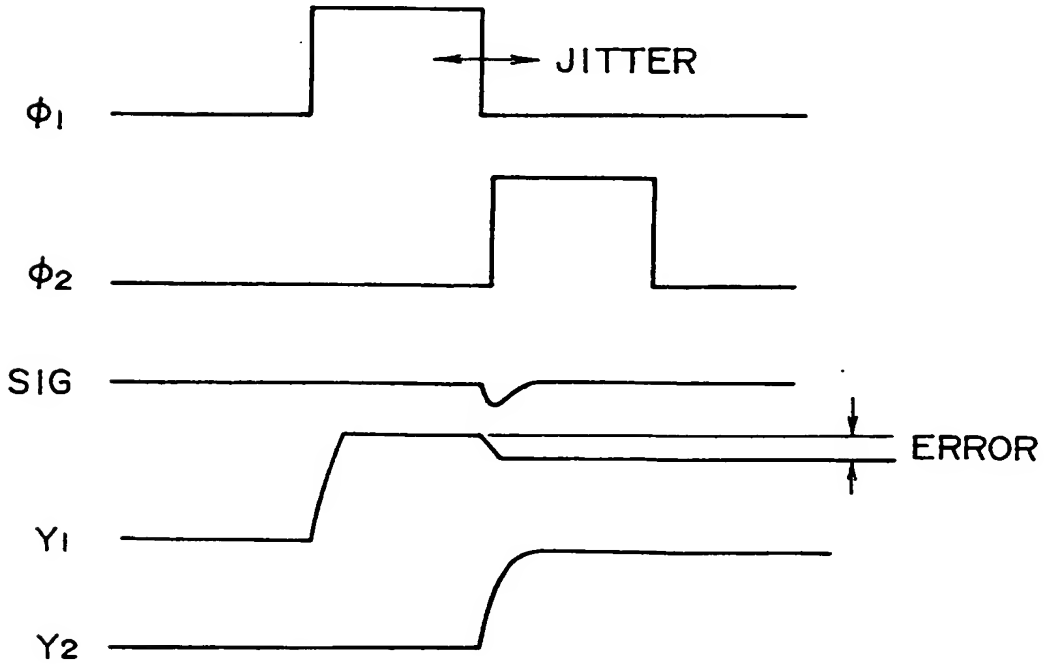

HCLK
HORIZONTAL SCANNING CIRCUIT
Φ1
Φ2
SIG
S1
S2
COM
L11
L12
T11
T12
X1
COM
L21
L22
T21
T22
X2
Y1
Y2

FIG. 9


JITTER
Φ1
Φ2
SIG
ERROR
Y1
Y2